Hard | Assistant Engineer (Electrical), Clas | 2025 | Building Department

The number of idle states (Ti), that is allowed between two INTA cycles, to meet the 8259A speed and cascade address output delay is

A 1

B 2

C **3** Correct

D 4

Correct Answer: C

Full Detailed Explanation

Open the live question URL below to read the full explanation, related links and practice flow.

Open live question on website:

https://sarkariresultout.com/pyq/hi/question/gpsc-ae-electrical-q225-idle-states-between-inta-cycles/