Hard | Assistant Engineer (Electrical), Clas | 2025 | Building Department

How the sag at higher stages can be reduced in a voltage multiplier circuit?

A. By decreasing the capacitance in the higher stages

B. By decreasing the capacitance in the lower stages

C. **By increasing the capacitance in the higher stages** — Correct

D. By increasing the capacitance in the lower stages

Correct Answer: C

Full Detailed Explanation

Open the live question URL below to read the full explanation, related links and practice flow.

Open live question on website:

https://sarkariresultout.com/pyq/gu/question/gpsc-ae-electrical-q229-voltage-multiplier-sag-reduction/