

Easy

Assistant Engineer (Electrical), Class 2025

Building Department

A 4-bit shift register that receives 4 bits of parallel data will shift to the _____ by _____ position for each clock pulse.

A

Right, one

Correct

B

Right, two

C

Left, one

D

Left, three

Correct Answer: A

Full Detailed Explanation

Open the live question URL below to read the full explanation, related links and practice flow.

Open live question on website:

<https://sarkariresultout.com/pyq/gu/question/gpsc-ae-electrical-q164-parallel-load-shift-register/>