Hard | Assistant Engineer (Electrical), Clas | 2025 | Building Department

The number of idle states (Ti), that is allowed between two INTA cycles, to meet the 8259A speed and cascade address output delay is

A 1

B 2

C **3** Correct

D 4

Correct Answer: C

Full Detailed Explanation

Concept & ReasoningCascaded 8259A systems use interrupt-acknowledge bus cycles to identify the requesting level and supply the vector information. Timing margins are inserted so internal priority resolution and cascade signals become valid before the next acknowledge phase. This is a hardware-interface timing fact specific to the 8259A/processor bus combination.How to Solve It in the Exam8259A timing questions are datasheet/protocol facts; don’t derive them from CPU frequency alone.Important Exam PointKeep cascade delay in mind when counting idle states.Related Revision PathThis question sits in the revision path Microprocessors and Interfacing 8259A PIC Interrupt Acknowledge .

Open live question on website:

https://sarkariresultout.com/pyq/question/gpsc-ae-electrical-q225-idle-states-between-inta-cycles/