Moderate | Assistant Engineer (Electrical), Clas | 2025 | Building Department

If the zeroth condition is satisfied then, for execution, the JNZ instruction takes

A 1 clock cycle

B 2 clock cycles

C 3 clock cycles

D **4 clock cycles** Correct

Correct Answer: D

Full Detailed Explanation

Concept & ReasoningConditional-branch timing must be read together with the exact processor architecture because 8085, 8086 and later x86 devices use different timing units and instruction encodings. The conceptual rule remains: JNZ means 'jump if not zero', so Z=1 means the branch condition is false; only the fall-through path executes. The official answer should be retained with that timing convention.How to Solve It in the ExamDecode the flag condition before recalling cycle counts.Important Exam PointDo not transfer timing numbers from one processor family to another.Related Revision PathThis question sits in the revision path Microprocessors and Interfacing Microprocessor Instructions Conditional Branching .

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