Easy | **Assistant Engineer (Electrical), Clas** | **2025** | **Building Department**

A 4-bit shift register that receives 4 bits of parallel data will shift to the _________ by _________ position for each clock pulse.

A **Right, one** — **Correct**

B Right, two

C Left, one

D Left, three

Correct Answer: A

Full Detailed Explanation

Concept & ReasoningParallel loading determines how the initial 4-bit word enters; it does not mean four positions shift at once. During serial shift operation, every active clock moves each stored bit to the adjacent stage by one position. Direction is set by the register configuration/control input.How to Solve It in the ExamParallel load parallel shift.Important Exam PointRead the direction stated/assumed by the device before tracing bits.Related Revision PathThis question sits in the revision path Digital Electronics Sequential Logic Shift Registers .