Easy | Deputy Executive Engineer (Electric | 2026 | orts Authority of Gujarat / Assistant Engineer (El

Consider the following statements regarding Memory interfacing in 8051: 1. Address decoding is required for memory interfacing. 2. Chip select signal is used to

A 1 and 2 only

B **1, 2 and 3** Correct

C 1 and 3 only

D 2 and 3 only

Correct Answer: B

Full Detailed Explanation

Correct Answer: B - 1, 2 and 3 Quick Concept Explanation The classic 8051 is an 8-bit Harvard-style microcontroller with separate code and data spaces. The standard core has 4 KB on-chip program ROM and 128 bytes internal RAM, supports external memory, multiple interrupts and configurable interrupt priority. Key relation: Reset SP=07H; classic internal RAM=128 bytes; standard ROM=4 KB.Exam focus: Remember 07H for stack pointer reset. Common trap: 00H is not the reset value of the 8051 stack pointer. Statement-wise Verification Statement 1 - Correct.Address decoding is required for memory interfacing.The standard core has 4 KB on-chip program ROM and 128 bytes internal RAM, supports external memory, multiple interrupts and configurable interrupt priority. Statement 2 - Correct.Chip select signal is used to enable memory device.The standard core has 4 KB on-chip program ROM and 128 bytes internal RAM, supports external memory, multiple interrupts and configurable interrupt priority. Statement 3 - Correct.Multiple devices can share data bus.The classic 8051 is an 8-bit Harvard-style microcontroller with separate code and data spaces. Core Concept The classic 8051 is an 8-bit Harvard-style microcontroller with separate code and data spaces. The standard core has 4 KB on-chip program ROM and 128 bytes internal RAM, supports external memory, multiple interrupts and configurable interrupt priority. On reset the